

*What is claimed is:*

1           1.     An apparatus for instruction-level parallelism in a processing element,  
2 comprising:

3           an instruction control unit;  
4           a first instruction buffer coupled to said instruction control unit;  
5           a second instruction buffer coupled to said instruction control unit;  
6           a dependency counter coupled to said instruction control unit;  
7           an execution switch coupled to said instruction control unit, said first instruction buffer,  
8 and said second instruction buffer; and  
9           an execution unit coupled to said execution switch.

1           2.     The apparatus of claim 1, wherein said dependency counter includes a first  
2 counter associated with the first instruction buffer and a second counter associated with the  
3 second instruction buffer.

1           3.     The apparatus of claim 1, wherein said instruction control unit identifies  
2 instruction dependency bits in said first instruction buffer, the instruction dependency bits being  
3 associated with instructions.

1           4.     The apparatus of claim 1, said instruction control unit generating control signals  
2 based on the dependency bits and values included in said dependency counter.

1           5.     The apparatus of claim 4, said execution switch providing instructions from said  
2 first instruction buffer to said execution unit based on control signals from said instruction  
3 control unit.

1           6.     The apparatus of claim 1, said execution switch providing instructions from said  
2 first instruction buffer to said execution unit based on control signals from said instruction  
3 control unit.

1           7.     An apparatus for processing instructions in multiple threads in an execution unit,  
2 comprising:

3           an instruction buffer holding a first instruction and a second instruction, the first  
4 instruction being associated with a first thread, and the second instruction being associated with a  
5 second thread;

6           a dependency counter;

7           an instruction control unit coupled to said instruction buffer and said dependency counter,  
8 said instruction control unit detecting instruction dependency bits and incrementing and  
9 decrementing said dependency counter; and

10          an execution switch coupled to said instruction control unit and said instruction buffer,  
11 said execution switch sending instructions to the execution unit.

1           8.     The apparatus of claim 7, wherein said dependency counter includes a first  
2 counter associated with the first thread and a second counter associated with the second thread.

1           9.     The apparatus of claim 7, wherein said instruction buffer includes the instruction  
2 dependency bits, the instruction dependency bits being associated with instructions.

1           10.    The apparatus of claim 7, wherein said instruction control detects dependency  
2 between the first instruction and the second thread based on dependency bits in said instruction  
3 buffer and a value of said dependency counter.

1           11.    The apparatus of claim 7, wherein said first processing element and said second  
2 processing element is disposed within a telecommunications switch.

1           12.    An apparatus for instruction-level parallelism, comprising:  
2 an instruction buffer holding a first instruction and a second instruction, the first  
3 instruction being associated with a first thread, and the second instruction being associated with a  
4 second thread; and  
5 an instruction control unit coupled to said instruction buffer, said instruction control unit  
6 detecting instruction dependency bits that indicate dependency between an instruction and one or  
7 more threads other than the thread with which the instruction is associated, and sending  
8 instructions to the execution unit to be executed.

1           13.    The apparatus of claim 12, wherein said instruction control unit identifies  
2 instruction dependency bits in said instruction buffer, the instruction dependency bits being  
3 associated with the first instruction and the second instruction.

1           14.    The apparatus of claim 12, wherein said instruction control detects dependency  
2   between the first instruction and the second instruction based on dependency bits in said  
3   instruction buffer.

1           15.    A method for processing instructions in multiple threads, comprising:  
2           receiving a first instruction associated with a first thread;  
3           determining that execution of the first instruction depends on execution of a second  
4   instruction, the second instruction being associated with a second thread;  
5           examining a counter associated with the first thread if said determining indicates that the  
6   first instruction depends on the execution of the second instruction;  
7           decrementing the counter if said examining indicates that the second instruction has  
8   already been executed; and  
9           executing the first instruction.

1           16.    The method of claim 15, further comprising suspending the processing of the first  
2   thread until said examining indicates that the second instruction has already been executed.

1           17.    A method for processing instructions in multiple threads, comprising:  
2           receiving a first instruction associated with a first thread;  
3           determining that execution of a second instruction depends on the execution of the first  
4   instruction, the second instruction being associated with a second thread;  
5           incrementing a counter associated with the second thread if said determining indicates  
6   that execution of a second instruction depends on the execution of the first instruction; and

7 executing the first instruction.

1 18. The method of claim 17, further comprising suspending the processing of the  
2 second thread if the counter associated with the second thread does not exceed a threshold.

1 19. A method for processing instructions in multiple threads, comprising:  
2 receiving a first instruction associated with a first thread;  
3 determining that the first instruction identifies a second thread;  
4 incrementing a counter associated with the second thread if said first instruction identifies  
5 the second thread;  
6 loading a second instruction associated with a second thread; and  
7 processing the second instruction in a manner related to the value of the counter  
8 associated with the second thread.

1 20. The method of claim 19, further comprising suspending the processing the second  
2 thread if the counter indicates that a dependent thread has not been executed.

1 21. The method of claim 19, further comprising executing the second instruction if  
2 the counter indicates that said first instruction has been executed.

1 22. A method for processing instructions in multiple threads, comprising:  
2 receiving a first instruction associated with a first thread;  
3 determining the first instruction identifies a second thread;

examining a counter associated with the second thread;  
decrementing the counter if said examining indicates a non-zero value; and  
executing the first instruction.

23. A method for processing instructions in multiple threads, comprising:  
loading a first instruction associated with a first thread;  
detecting dependency between the first instruction and a second instruction associated  
with a second thread based on dependency bits in an instruction buffer and the value of a  
dependency counter.

24. An apparatus for processing instructions in multiple threads, comprising:  
an instruction buffer configured to hold a first instruction and a second instruction, the  
first instruction including a dependency indicator and being associated with a first thread, and the  
second instruction including a dependency indicator and being associated with a second thread;  
an instruction control unit coupled to said instruction buffer;  
a dependency counter coupled to said instruction control unit, said dependency counter  
associated with the first thread;  
said instruction control unit configured to detect the dependency indicators and change  
the value of said dependency counter in response to detecting the dependency indicators; and  
said instruction control unit configured to disallow execution of the first instruction if  
said dependency counter includes a value less than a threshold value.

1           25.    The apparatus of claim 24, wherein said instruction control unit is configured to  
2   determine that the dependency indicator included in the first instruction indicates that the second  
3   thread includes an instruction on which the first instruction depends.

1           26.    The apparatus of claim 24, wherein the dependency indicator included in the first  
2   instruction is a depends bit.

1           27.    The apparatus of claim 24, wherein said instruction control unit is configured to  
2   determine that the dependency indicator included in the second instruction indicates that the first  
3   thread includes an instruction that is dependent on the second instruction.

1           28.    The apparatus of claim 24, wherein the dependency indicator included in the  
2   second instruction is a tells bit.

1           29.    The apparatus of claim 24, wherein said instruction control unit is configured to  
2   increment said dependency counter in response to detecting the dependency indicator included in  
3   the second instruction.

1           30.    The apparatus of claim 24, wherein said instruction control unit is configured to  
2   decrement said dependency counter in response to detecting the dependency indicator included  
3   in the first instruction.